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L2	L1 and gate with select$5 with signal	344	L2
L1	((345/$3).ccls.) and gate with line with driv$3	909	L1

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L16: Entry 1 of 1 File: EPAB Mar 22, 2000

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ABSTRACT:

Brief Summary Text (25):
To achieve the aforementioned object, a display driving apparatus according to a further aspect of this invention comprises a display panel having a plurality of display elements laid out on a substrate in a predetermined pattern; a data side driver section, formed on the substrate, for supplying data to the display elements, the data side driver section having a plurality of groups each including a plurality of data side drivers; a column of data lines arranged in parallel and each connected to a plurality of display elements and connected to a same data side driver with (r.multidot.S-1) data lines, connected to other data side drivers, in between, where r is the number of the groups and S is the number of data side drivers in the same group; a scan side driver for scanning the display elements by a plurality of numbers; a plurality of scan lines for each connecting a plurality of display elements to the scan side driver; and clock signal supply means for supplying a common clock signal to an associated one of the data side driver in each of the groups.

Detailed Description Text (5):
In FIG. 2, a display driving apparatus 20 comprises a circuit-integrated type active matrix LC display panel 33, which has an active matrix array 22, a single gate line driver 23 as a scan side driver and nine drain line drivers 24, 25, 26, 27, 28, 29, 30, 31 and 32 as data side drivers all formed on a substrate 21, and an external circuit 34.

Detailed Description Text (6):
The active matrix array 22 has a plurality of gate lines GL1-GLm and a plurality of drain lines DL1-DLn formed in a matrix form on the substrate 21. Display elements each comprising a TFT as a switching element and a pixel LC are arranged in association with the individual intersections between the gate lines GL1-GLm and the drain lines DL1-DLn. FIG. 2 which shows only one of the display elements. In FIG. 2 the gate and drain of a TFT are connected to the vicinity of the intersection of one gate line GL and its associated drain line DL, with the pixel LC connected to the source of the TFT.

Detailed Description Text (8):
The individual gate lines GL1-GLm are connected to the gate line driver 23, which receives a G-clock signal from a controller (not shown). Based on the G-clock signal, the gate line driver 23 sequentially outputs gate signals to the individual gate lines GL1-GLm to sequentially select the gate lines GL1-GLm, thus turning on the TFTs connected to the selected gate lines GL1-GLm.

Detailed Description Text (9):
The data side driver section comprising the nine drain line drivers 24-32 formed on the substrate 21 is separated into three groups G1, G2 and G3 respectively consisting of the drain line drivers 24-26, the drain line drivers 27-29 and the drain line drivers 30-32. Each of the drain lines DL1-DLn is connected one of the three drain line drivers 24-26, 27-29 or 30-32 in the group G1, G2 or G3, so that the drain lines DL1-DLn are segmented to nine driving sections.

Detailed Description Text (10):
More specifically, the drain lines DL1-DLn are separated into three driving sections, drain lines DL1-DLp, data lines DLp+1-DLq and data lines DLq+1-DLn equal in number counting from the leftmost line in FIG. 2. The drain lines DL1-DLp, data lines DLp+1-DLq and data lines DLq+1-DLn in those driving sections are connected one to one to the associated drain line drivers 24-26 in the group G1, drain line drivers 27-29 in the group G2 and drain line drivers 30-32 in the group G3, so that each driving section is further divided into three sub driving sections.

Detailed Description Text (12):
More specifically, the drain line DL1 among the drain lines DL1-DLp is connected to the drain line driver 24 in the group G1 consisting of the drain line drivers 24-26, the drain line DL2 to the drain line driver 25, and the drain line DL3 to the drain line driver 26. Likewise, the next set of drain lines are respectively connected to the drain line drivers 24 to 26 in the group G1. Finally, the drain line DLp-2 is connected to the drain line driver 24, the drain line DLp-1 to the drain line driver

25, and the drain line DLp to the drain line driver 26. Likewise, the data lines DLp+1-DLq are connected to the associated drain line drivers 27-29 in the group G2, and the data lines DLq+1-DLn are connected to the associated drain line drivers 30-32 in the group G3.

Detailed Description Text (14):
Thinned video signals V.sub.A, V.sub.B and V.sub.C, which will be discussed later, are input from the external circuit 34 to the drain line drivers 24-26 in the group G1, the drain line drivers 27-29 in the group G2 and the drain line drivers 30-32 in the group G3, group by group, via data signal lines L.sub.1, L.sub.2 and L.sub.3. Further, a clock signal CT1 is input to the associated drain line drivers 24, 27 and 30 in the groups G1, G2 and G3 via a clock signal line L.sub.4, a clock signal CT2 is input to the associated drain line drivers 25, 28 and 31 in the groups G1, G2 and G3 via a clock signal line L.sub.5, and a clock signal CT3 is input to the associated drain line drivers 26, 29 and 32 in the groups G1, G2 and G3 via a clock signal line L.sub.6.

Detailed Description Text (16):
Referring to FIG. 3, each of the drain line drivers 24-32 comprises three shift registers 41 to 43, 44 to 46 or 47 to 49, nine in total, transfer gates TG1 to TGp, TGp+1 to TGq or TGq+1 to TGn connected between the shift registers 41-43, 44-46 or 47-49 and the associated data lines DL1-DLn, and inverters I1 to Ip, Ip+1 to Iq or Iq+1 to In each connected to one control terminal of the associated one of the transfer gates TG1-TGp, TGp+1-TGq or TGq+1-TGn. A horizontal sync signal .phi.H is input to the individual shift registers 41-49. The clock signal CT1 is input to the associated shift registers 41, 44 and 47 in the groups G1, G2 and G3, the clock signal CT2 is input to the associated shift registers 42, 45 and 48 and the clock signal CT3 is input to the associated shift registers 43, 46 and 48.

Detailed Description Text (17):
The transfer gates TG1-TGp, TGp+1-TGq or TGq+1-TGn respectively connected to the shift registers 41-43, 44-46 and 47-49 in the groups G1, G2 and G3 have their input terminals connected to the associated data signal lines L.sub.1 to L.sub.3, and their output terminals connected to the associated data lines DL1-DLn. The thinned video signals V.sub.A, V.sub.B and V.sub.C to be discussed shortly are respectively input to the input terminals of those transfer gates TG1-TGp, TGp+1-TGq or TGq+1-TGn.

Detailed Description Text (18):
The individual shift registers 41-49 shift data, set based on the horizontal sync signal .phi.H, by one bit in accordance with the falling of the associated clock signal CT1, CT2 or CT3, and send their outputs (bit data) as control signals .phi.1, .phi.2, .phi.3, . . . from the output terminals to the control terminals of the transfer gates TG1-TGp, TGp+1-TGq or TGq+1-TGn connected to those output terminals. The control signals .phi.1, .phi.2, and so forth are input directly to one control terminals of the transfer gates TG1-TGp, TGp+1-TGq and TGq+1-TGn and are input to the other control terminals after being inverted by the respective inverters I1-In. In response to the control signals from the associated shift registers 41-49, the transfer gates TG1-TGp, TGp+1-TGq or TGq+1-TGn are enabled to supply the thinned video signals V.sub.A, V.sub.B and V.sub.C input then onto the associated data lines DL1-DLn.

Detailed Description Text (20):
In synchronism with the D-clock signal, the shift register 51 causes the sample and hold circuit 52 to sample and hold the input analog video signal DATA. When the scanning of the next scan line starts, the video signals written in the sample and hold circuit 52 are transferred to the sample and hold circuit 53, for example, in response to a horizontal sync signal .phi.H. The thinned video signals written in this sample and hold circuit 53 are divided to one third of one scan line each by the shift registers 54, 55 and 56 which transfer drive signals in synchronism with the output signal of the counter 57, and the divided video signals are output in parallel to the drain line drivers 24-26, 27-29 and 30-32 of the groups G1, G2 and G3 as thinned video signal data V.sub.A, V.sub.B and V.sub.C.

Detailed Description Text (24):

The shift register 51 causes video signals DATA to be sequentially written and held in the sample and hold circuit 52 in synchronism with the D-clock signal as shown in FIGS. 4A and 4B. When the scanning of the next gate line starts, the video signals DATA written in the sample and hold circuit 52 are transferred to the sample and hold circuit 53. As mentioned above, the display driving apparatus 20 comprises the substrate 21, the active matrix array 22 formed on the substrate 21, the gate line driver 23 and the nine drain line drivers 24-32. The individual data lines DL1-DLn of the active matrix array 22 are connected in order to the drain line drivers 24-26, the drain line drivers 27-29 and the drain line drivers 30-32 in the groups G1, G2 and G3 each consisting of three drain line drivers, so that those data lines are separated into nine driving sections. The first thinned video signals V.sub.A shown in FIG. 4D, obtained by trisecting one horizontal scan line of analog video signals, are commonly input to the drain line drivers 24-26 in the group G1. The second thinned video signals V.sub.B shown in FIG. 4E, another trisected analog video signals, are likewise commonly input to the drain line drivers 27-29 in the group G2. Further, the third thinned video signals V.sub.C shown in FIG. 4F, another trisected analog video signals, are commonly input to the drain line drivers 30-32 in the group G3.

Detailed Description Text (28):
The thinned video signals V.sub.A of analog video signals DATA having data A1, A2, A3, . . . for the first 1/3 period of each horizontal scanning period are held in the sample and hold circuit 53, and thinned video signals V.sub.A consisting of thinned data V.sub.A1, V.sub.A2, V.sub.A3, . . . corresponding to the held signals are transferred to the drain line drivers 24, 25 and 26 in synchronism with the output signal of the counter 57. The first video signal V.sub.A1 among the thinned video signals V.sub.A transferred to the drain line driver 24 is supplied via the transfer gates TG1 to the data line DL1 when the control signal .phi.1 becomes an H level in response to the falling of the clock signal CT1 which is the D-clock signal frequency-divided to one ninth as shown in FIGS. 4G and 4H. In response to next falling of the clock signal CT1, the data in the shift register 41 is shifted by one bit and the control signals .phi.1 and .phi.4 become an L level and H level, respectively, as shown in FIGS. 4G, 4H, and 4I, closing the transfer gates TG1 and opening the transfer gate TG4. The video signal V.sub.A1 which has been applied immediately before closing of the transfer gates TG1 is held in the pixel capacitor LC and the floating capacitor of the data line DL1.

Detailed Description Text (29):
Next, the second video signal V.sub.A2 among the thinned video signals V.sub.A transferred to the drain line driver 25 is supplied to the data line DL2 via the transfer gates TG2, which is opened when the control signal .phi.2 became an H level, in response to the clock signal CT2 which is the D-clock signal frequency-divided to one ninth and has a phase delay of 120 degrees from the clock signal CT1, as shown in FIGS. 4J and 4K. When the clock signal CT2 falls next, the control signal .phi.2 becomes an L level, as shown in FIGS. 4J and 4K, closing the transfer gates TG2. Consequently, the video signal V.sub.A2 which has been applied when the transfer gates TG2 has been closed, is held in the pixel capacitor LC and the floating capacitor of the data line DL2.

Detailed Description Text (30):
The third video signal V.sub.A3 among the thinned video signals V.sub.A transferred to the drain line driver 26 is supplied to the data line DL3 via the transfer gates TG3, which were opened when the control signal .phi.3 became an H level, in response to the clock signal CT3 which is the D-clock signal frequency-divided to one ninth and has a phase delay of 120 degrees from the clock signal CT2, as shown in FIGS. 4L and 4M. When the clock signal CT3 falls next, the control signal .phi.3 becomes an L level, as shown in FIGS. 4L and 4M, closing the transfer gates TG3. Consequently, the video signal V.sub.A3 is held in the pixel capacitor LC and the floating capacitor of the data line DL3.

Detailed Description Text (31):
In this manner, the drain line driver 24 supplies the thinned video signals V.sub.A to the data lines DL1, DL4, . . . , DLp-2 in response to the clock signal CT1 which is the D-clock signal frequency-divided to one ninth. The drain line driver 25 supplies the thinned video signals V.sub.A to the data lines DL2, DL5, . . . , DLp-1

in response to the clock signal CT2 which is the D-clock signal frequency-divided to one ninth and has a phase delay of 120 degrees from the clock signal CT1. The drain line driver 26 supplies the thinned video signals V.sub.A to the data lines DL3, DL6, . . . , DLp in response to the clock signal CT3 which is the D-clock signal frequency-divided to one ninth and has a phase delay of 120 degrees from the clock signal CT2. The video signals V.sub.A supplied to each data line DL is held by the capacitor between that data line DL and the substrate 21 and the pixel capacitor LC, and is held in the pixel capacitor LC after the associated TFT in the active matrix array 22 is turned off, in response to turning off of the gate pulse.

Detailed Description Text (33):
For the group G2, the drain line driver 27 supplies the thinned video signals V.sub.B to the data lines DLp+1, DLp+4, . . . , DLq-2 in response to the clock signal CT1. The drain line driver 28 supplies the thinned video signals V.sub.B to the data lines DLp+2, DLp+5, . . . , DLq-1 in response to the clock signal CT2 having a phase delay of 120 degrees from the clock signal CT1. The drain line driver 29 supplies the thinned video signals V.sub.B to the data lines DLp+3, DLp+6, . . . , DLq in response to the clock signal CT3 having a phase delay of 120 degrees from the clock signal CT2.

Detailed Description Text (34):
With regard to the group G3, the drain line driver 30 supplies the thinned video signals V.sub.C to the data lines DLq+1, DLq+4, . . . , DLn-2 in response to the clock signal CT1. The drain line driver 31 supplies the thinned video signals V.sub.C to the data lines DLq+2, DLq+5, . . . , DLn--1 in response to the clock signal CT2 having a phase delay of 120 degrees from the clock signal CT1. The drain line driver 32 supplies the thinned video signals V.sub.C to the data lines DLq+3, DLq+6, . . . , DLn in response to the clock signal CT3 having a phase delay of 120 degrees from the clock signal CT2.

Detailed Description Text (35):
As mentioned above, the drain line drivers 24, 27 and 30 are driven by the common clock signal CT1. Therefore, the thinned video signals V.sub.A1, V.sub.B1 and V.sub.C1 are supplied to the respective data lines DL1, DLp+1 and DLq+1 and held in the respective pixel capacitors LC in the same scanning period, as shown in FIG. 4H. Likewise, the drain line drivers 25, 28 and 31 are driven by the common clock signal CT2. Therefore, the thinned video signals V.sub.A2, V.sub.B2 and V.sub.C2 are supplied to the respective data lines DL2, DLp+2 and DLq+2 and held in the respective pixel capacitors LC in the same scanning period, as shown in FIG. 4K. Further, the drain line drivers 26, 29 and 32 are driven by the common clock signal CT3. Therefore, the thinned video signals V.sub.A3, V.sub.B3 and V.sub.C3 are supplied to the respective data lines DL3, DLp+3 and DLq+3 and held in the respective pixel capacitors LC in the same scanning period, as shown in FIG. 4M.

Detailed Description Text (36):
A gate pulse turns on, for example, before the control signal .phi.1 turns on, and turns off after last thinned video signals are supplied to the respective data lines and held in the respective pixel capacitors.

Detailed Description Text (38):
The individual data lines DL1-DLn are connected one to one to the drain line drivers 24-26, the drain line drivers 27-29 and the drain line drivers 30-32. Therefore, the data lines DL1-DLn are separated into the driving sections equal in number (3) to the groups G1, G2 and G3. The associated sets of the drain line drivers 24-26, the drain line drivers 27-29 and the drain line drivers 30-32 in the groups G1, G2 and namely, the drain line drivers 24, 27 and 30, the drain line drivers 25, 28 and 31, and the drain line drivers 26, 29 and 32, are connected by their common clock signal lines. The drain line drivers 24-26, the drain line drivers 27-29 or the drain line drivers 30-32 in the group G1, G2 or G3 are respectively driven by the clock signals CT1, CT2 and CT3 whose phases are shifted from one another by the angle corresponding to the number of the drain line drivers constituting each group G1, G2 or G3 (three drivers in this embodiment).

Detailed Description Text (39):
Accordingly, the frequency of the clock signals CT1, CT2 and CT3 can be reduced in

inverse proportion to the product of the number of the groups of the data side driver section (the number of the driving sections) and the number of the drain line drivers constituting each group. Even if slow switching elements, such as polysilicon-based TFTs, are used for the drivers, therefore, it is possible to ensure a sufficient driving speed to cope with display panels having high definition and large screen. Accordingly, even display panels having high-pixel capacitance, such as HDTVs can provide high-quality images.

Detailed Description Text (41):
In FIG. 5, a display driving apparatus 70 comprises a circuit-integrated type active matrix LC display panel 83, which has a substrate 71, an active matrix array 72, a single gate line driver 73 and nine drain line drivers 74, 75, 76, 77, 78, 79, 30, 81 and 82 all formed on the substrate 71, and an external circuit 84.

Detailed Description Text (42):
The active matrix array 72 has a plurality of gate lines GL1-GLm and a plurality of drain lines DL1-DLn formed in a matrix form on the substrate 71. Display elements each consisting of a TFT as a switching element and a pixel LC are arranged at the individual intersections between the gate lines GL1-GLm and the drain lines DL1-DLn. In FIG. 5 which shows only one of the display elements, the gate and drain of a TFT are connected to the vicinity of the intersection of one gate line GL and its associated drain line DL, with the pixel LC connected to the gate of the TFT.

Detailed Description Text (43):
The individual gate lines GL1-GLm are connected to the gate line driver 73, which receives a G-clock signal from a controller (not shown).

Detailed Description Text (44):
Based on the G-clock signal, the gate line driver 73 sequentially outputs gate signals to the individual gate lines GL1-GLm to selectively scan the gate lines GL1-GLm one by one, thus turning on the TFTs connected to the selected gate lines GL1-GLm.

Detailed Description Text (45):
The video signals to be input to the drain line drivers 74-82 are separated into groups as will be discussed later. Therefore, the data side driver section comprising the nine drain line drivers 74-82 formed on the substrate 71 are separated into three groups G1, G2 and G3 respectively consisting of the drain line drivers 74-76, the drain line drivers 77-79 and the drain line drivers 80-82. Each of the drain lines DL1-DLn is connected to one of the individual drain line drivers 74-76, 77-79 or 80-82 in the group G1, G2 or G3, so that the drain lines DL1-DLn are segmented to nine driving sections.

Detailed Description Text (50):
Though not illustrated, each of the drain line drivers 74-82 comprises three shift registers, nine in total, transfer gates connected between the shift registers and the associated data lines DL1-DLn, and inverters each connected to one control terminal of the associated one of the transfer gates, as per the first embodiment. A horizontal sync signal is input to the individual shift registers from a display controller (not shown). The clock signals CT1, CT2 and CT3 are respectively input to the shift registers of the associated drain line drivers 74-82 in the groups G1, G2 and G3.

Detailed Description Text (52):
The shift registers of the individual drain line drivers 74-82 shift bit data, set based on the horizontal sync signal, in response to the associated clock signals CT1, CT2 and CT3, and send their outputs as control signals from the output terminals. Those output control signals are input directly to one control terminals of the transfer gates and are input to the other control terminals after being inverted by the respective inverters. In response to the control signals from the associated shift registers, the transfer gates are enabled to supply the serial thinned video signals V.sub.A, V.sub.B and V.sub.C input then onto the associated drain lines DL1-DLn.

Detailed Description Text (57):

The shift registers 95, 96 and 97 divide the thinned video signals output from the multiplexer 94 one third of one scan line in a predetermined order, based on the 1/3-frequency-divided clock from the counter 98. The trisected signals are output as serial thinned video data V.sub.A, V.sub.B and V.sub.C to the drain line drivers 74-76, 77-79 and 80-82 in the groups G1, G2 and G3 in parallel.

Detailed Description Text (60):
The aforementioned one scan line of thinned video signal are output by the shift register 96 as the fourth to sixth sampled thinned video signals B1, B2 and B3 and three consecutive thinned video signals starting from every ninth one thereafter, as serial thinned video data V.sub.B1, V.sub.B2, V.sub.B3, V.sub.B4, V.sub.B5, V.sub.B6, . . . to the drain line drivers 77-79 in the group G2.

Detailed Description Text (61):
Further, the aforementioned one scan line of thinned video signals are output by the shift register 97 as the seventh to ninth sampled thinned video signals C1, C2 and C3 and three consecutive thinned video signals starting from every seventh one thereafter, as serial thinned video data V.sub.C1, V.sub.C2, V.sub.C3, V.sub.C4, V.sub.C5, V.sub.C6, . . . to the drain line drivers 80-82 in the group G3.

Detailed Description Text (64):
As described above, the shift registers 95-97 separate the thinned video signals output from the multiplexer 94 to one third of one scan line in the aforementioned order and output the resultant signals in parallel as serial thinned video data V.sub.A, V.sub.B and V.sub.C shown in FIGS. 6D, 6E, and 6F to the drain line drivers 74-76, 77-79 and 80-82 in the groups G1, G2 and G3.

Detailed Description Text (68):
The display driving apparatus 70 has the substrate 71, the active matrix array 72, the gate line driver 73 and the nine drain line drivers 74-82 all formed on the substrate 71, as mentioned earlier. The individual data lines DL1-DLn of the active matrix array 72 are connected one to one to the drain line drivers 74-76, the drain line drivers 77-79 and the drain line drivers 80-82 every three drivers constituting one group, so that the data lines DL1-DLn are separated into nine driving sections.

Detailed Description Text (69):
The serial thinned video signals V.sub.A shown in FIG. 6D, which consists of the first sampled consecutive thinned video signals among the analog video signals DATA and every three consecutive thinned video signals sampled starting from every ninth one thereafter, are commonly input to the drain line drivers 74-76 in the group G1. Likewise, the serial thinned video signals V.sub.B shown in FIG. 6E, which consists of the fourth to sixth sampled consecutive thinned video signals among the analog video signals DATA and every three consecutive thinned video signals sampled starting from every ninth one thereafter, are commonly input to the drain line drivers 77-79 in the group G2. Further, the serial thinned video signals V.sub.C shown in FIG. 6F, which consists of the seventh to ninth sampled consecutive thinned video signals among the analog video signals DATA and every three consecutive thinned video signals sampled starting from every ninth one thereafter, are commonly input to the drain line drivers 80-82 in the group G3.

Detailed Description Text (72):
One scan line of thinned video signals consisting of signals A1, A2, A3, B1, B2, B3, C1, C2, C3, . . . are held and sampled in the sample and hold circuit 92. The sampled video signals are then supplied to the multiplexer 94. The multiplexer 94 rearranges the received video signals to A1-An, B1-Bn, C1-Cn. Every ninth output of the multiplexer 94 is selected by the shift registers 95, 96 and 97, and the resultant video signals are transferred as the serial thinned video data V.sub.A1, V.sub.A2, V.sub.A3 ; V.sub.B1, V.sub.B2, V.sub.B3 ; V.sub.C1, V.sub.C2, V.sub.C3 ; and so forth to the drain line drivers 74-76 in the group G1; the drain line drivers 77-79 in the group G2; and the drain line drivers 80-82 in the group G3 in synchronism with the output signal of the counter 98.

Detailed Description Text (73):
Let us now consider the group G1 consisting of the drain line drivers 74-76. The first video signal V.sub.A1 among the serial thinned video signals V.sub.A

transferred to the drain line driver 74 is supplied to the data line DL1 via the transfer gate which opens and closes in synchronism with the falling of the clock signal CT1, which is the D-clock signal frequency-divided to one ninth.

CLAIMS:

1. A display driving apparatus comprising:

a display panel having a plurality of display elements laid out on a substrate in a predetermined pattern;

a data side driver section, formed on said substrate, for supplying data to said display elements, said data side driver section having a plurality of groups each including a plurality of data side drivers;

a column of data lines arranged in parallel, each of said data lines being connected to a plurality of display elements and to one of said data side drivers which is associated with a position of a column of said connected display elements;

a scan side driver for scanning said display elements;

a plurality of scan lines, each for connecting a plurality of display elements to said scan side driver;

clock signal supply means for generating a plurality of common clock signals whose phases are shifted from each other, and for supplying different common clock signals to each group of data side drivers and each of the different clock signals being applied to corresponding data side drivers in each of said groups; and

data signal supply means for supplying a common data signal to all of said data side drivers in each of said groups, group by group, said data signal supply means having a plurality of data signal lines respectively connected to all of said data side drivers in each of said groups.

3. The display driving apparatus according to claim 2, wherein the number of data side drivers in a group is S, and individual data lines in said column of data lines are connected to a same data side driver with (S-1) data lines, connected to other data side drivers in a same group, in between.

4. The display driving apparatus according to claim 1, wherein the number of said groups is r and the number of data side drivers in a group is S, and individual data lines in said column of data lines are connected to a same data side driver with (r.multidot.S-1) data lines, connected to other data side drivers, in between.

6. The display driving apparatus according to claim 1, wherein said clock signal supply means has a plurality of clock signal lines connected to associated data side drivers in each of said groups.

9. The display driving apparatus according to claim 1, wherein said data signal supply means includes a data signal generator for separating one scan line of input video signals in accordance with the number of said groups and for respectively supplying said separated video signals to said data signal lines.